REMARKS

In the January 11, 2005 Office Action, claims 1-5 were rejected under 35 U.S.C. § 103(a). Claims 1-5 remain in the case. Claim 1 is herein amended and new claims 6-9 are added in this Amendment After Final, to clarify salient features of the claimed invention. No new matter has been added. Claims 1-9 are pending. The rejections are traversed below.

This Amendment After Final addresses the Examiner's rejections to claims 1, 4, and 5 under 35 U.S.C. § 103(a) as being unpatentable over Ahmad et al. (USP 5,209,817) and the Examiner's rejections to claims 2, and 3 under 35 U.S.C. § 103(a) as being unpatentable over Ahmad in view of Masahiro et al. (reference AH cited in PTO-1449) and the Examiner's rejections to claims 1-5 under 35 U.S.C. § 103(a) as being unpatentable over Lin et al. (Pub. No.: US 2004/0166659) in view of Ahmad.

The Application

The application relates to a basic manufacturing process of forming wiring for electronic parts such as semiconductor wafers or substrates. As illustrated in Fig. 1(a), a first insulating layer 41 is formed on a surface of a substrate 40. The first insulating layer 41 is hardened. Then as illustrated in Fig. 1(b), a second insulating layer 42 is formed on top of the hardened first insulating layer 41. Then as illustrated in Fig. 1(c), the second insulating layer 42 is exposed and developed to form pattern groove 44; where the bottom face of pattern groove 44 is formed of the exposed portion of the top face of insulating layer 41, and the sidewall inner surfaces of pattern groove 44 are formed of the exposed and developed sidewall surfaces of insulating layer 42 (refer to Fig. 1(c)); (NOTE: The term "sidewall(s)" corresponds to the "inner faces of the pattern groove 44" described in the specification at page 8, lines 32-33). Next, as illustrated in Fig. 1(d), seed layer 46 used for plating is formed contiguously on the surfaces of the second insulating layer 42 and pattern groove 44, including the sidewall inner faces of pattern groove 44 and the exposed portion of the top face of insulating layer 41 which is the bottom face of pattern groove 44. Next, as illustrated in Fig. 1(e), photosensitive resist is coated only on the surface of the seed layer horizontally adjacent to the top surface of the second insulating layer 42, leaving the seed layer surfaces defined by the surfaces of pattern groove 44 exposed and not covered by the photosensitive resist coating. Next as illustrated in Fig. 1(f), conductor 52 is formed in the pattern groove 44 by first heaping copper plating layer 50 into the pattern groove 44 up to the same thickness as the thickness of the second insulating layer 42 , then in order following the heaping of copper into pattern groove 44, a barrier layer 51 of nickel plating is formed in the pattern groove 44 on top of the heaped copper plating layer 50. Next as illustrated in Fig. 1(g),

the photosensitive resist 48 is removed exposing the surface of seed layer 46 that is horizontally adjacent to the top surface of second insulating layer 42. Finally, as illustrated in Fig. 1(h), seed layer 46 horizontally adjacent to the top surface of the second insulating layer 42 is removed by etching thus forming wiring pattern 52a. The thickness of seed layer 46 is much smaller than the thickness of the conductor 52, and the side portions of conductor 52 are protected by the second insulating layer 42; therefore, when the seed layer 46 is removed by etching, conductor 52 is not eroded by the etchant, and the formation accuracy of the wiring pattern 52a is maintained.

The Applied Art:

U.S. Patent 5,209,817 Ahmad et al.

The Ahmad patent is directed to a method of "constructing vias and wiring in a single composite level ... which does not require the use of a photosensitive polyimide base material ... this invention contemplates the provision of a multi-level wiring structure in which wires and vias are formed by an isotropic deposition of a conductive material, such as copper, on a dielectric base .... In a preferred embodiment of the invention copper is electroplated to a thin seed conducting layer deposited on the surface of the dielectric base in which via openings have been formed. Openings in a resist formed on the surface of the dielectric base over the seed layer form a pattern defining the wiring and via conductor features. Electroplated copper fills the via openings and wire pattern openings in the resist isotropically so that the upper surfaces of the wiring and vias are co-planar when the plating step is complete." (See Ahmad (col. 1, ll. 45-68; col. 2, ll. 1-15; FIG. 6 and FIG. 7)).

Japanese Patent Abstract 2001-053075 Masahiro et al.

The Masahiro patent is directed to a method of constructing vias and wiring where "A via hole is provided on insulating layers 11 and 13, a metal thin film 14 is formed covering the insulating layer 13 and a lower conductor layer 12 so as to be electrically connected to the lower conductor layer 12 through the intermediary of the vial hole, a wiring layer 17 is formed on the metal thin film 14, and the surface of the metal thin film 14 is covered with a coating layer 18 .... It is preferable that nickel/gold, nickel/palladium or nickel/palladium/gold is used as the ... coating layer 18. (See Masahiro (the ABSTRACT; and figures)). NOTE: Only a translated ABSTRACT of the Masahiro patent has been provided by the PTO.

U.S. Patent Publication 2004/0166659 A1 Lin et al.

The Lin patent is directed to a method "where key re-distribution and interconnection metal layers and dielectric layers are added over a conventional IC." (See Lin (¶[0045])). "The

present invention adds one or more thick layers of polymer dielectric and one or more layers of thick wide metal lines on top of the finished device wafer passivation. The thick layer of dielectric can, for example, be of polyimide or benzocyclobutene (BCB) with a thickness of over, for example, 3 um. The wide metal lines can, for instance, be of electroplated copper or gold .... Single, dual and triple damascene techniques, or combinations thereof, are used for forming the metal lines and via fill." (See Lin (¶[0026])). "Where Cu is used for electroplating to form the structure of Fig. 12g, a nickel cap layer ... may be used to prevent copper corrosion and to prevent interaction of the copper with the surrounding polymer." (See Lin (¶[0054])).

ITEM 2: Rejection of claims 1, and 4-5 under 35 U.S.C. § 103(a) over Ahmad

In the January 11, 2005 Office Action, claims 1, and 4-5 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ahmad.

In contrast to the Ahmad patent which (as described in Ahmad (Figures 18 through 21)) is directed to constructing vias and wiring in both a first single "dielectric layer 10", as well as a second "resist layer 40", the instant application as discussed above in The Application section is directed to a manufacturing process of forming pattern grooves for wiring in only a second insulating layer which is positioned on top of a first hardened insulation layer. The January 11, 2005 Office Action asserts that the Ahmad reference shows "exposing and developing the second photosensitive insulating resin layer to form pattern grooves so that the first photosensitive polyimide layer is exposed at bottoms of the pattern grooves ...." However, Ahmad does not show the "light-exposing" element and limitations of claim 1, which as amended is recited below:

> light-exposing and developing the second insulating layer to form pattern grooves, each having sidewalls and a bottom so that the first insulating layer is exposed at the bottom of each pattern groove ...."

(claim 1, lines 5-7). Further review of Ahmad (Fig. 18) compared with Fig. 1(c) of the claimed invention shows that in Ahmad (Fig. 18), the bottom of the wiring pattern groove is not the top surface of the first insulating layer, i.e., not the top surface of "dielectric layer 10"; instead, the bottom of the wiring pattern groove in Ahmad is the "capture pad 40" as shown and referenced in Ahmad (Fig. 17) and only shown (not referenced) in Ahmad (Fig. 18).

The Office Action asserts that the Ahmad reference shows "forming a plating seed layer (42) on the second photosensitive insulating resin layer including inner surfaces of the pattern grooves ...." However, Ahmad does not show the "forming a plating seed layer" element and

limitations of claim 1, which as amended recites:

> forming a plating seed layer on the second insulating layer including inner surfaces of the pattern grooves and then forming a resist pattern on the plating seed layer except for portions of the pattern grooves of the second insulating layer so that the seed layer only on the sidewalls and the bottom of the pattern grooves is exposed ....

(claim 1, lines 8-11). Nothing has been cited in Ahmad defining the wiring pattern groove sidewalls and bottom characteristics where the first insulating layer is exposed at the bottom of each of the pattern grooves related to forming conductor wiring patterns in semiconductor wafers or substrates, because Ahmad does not contain such disclosure. The applied art fails to teach or suggest all of the limitations of the claimed invention; thus, the Office Action fails to establish a case of *prima facie* obviousness for independent claim 1 as being unpatentable over the single reference Ahmad.

Dependent claims 4-5 each depending from independent claim 1 are patentable over the applied art of record Ahmad for at least the same reasons that independent claim 1 is patentable over Ahmad. It is respectfully requested that the rejection of claims 1, and 4-5 under 35 U.S.C. § 103(a) as being unpatentable over Ahmad be withdrawn in the next Office Action.

ITEM 3: Rejection of claims 2-3 under 35 U.S.C. § 103(a) over Ahmad in view of Masahiro

Dependent claims 2-3 each depending from independent claim 1 are patentable over the applied art of record Ahmad in view of Masahiro for at least the same reasons that independent claim 1 is patentable over Ahmad, as discussed above. Furthermore, nothing has been cited in either Masahiro or Ahmad defining the wiring pattern groove sidewalls and bottom characteristics where the first insulating layer is exposed at the bottom of each of the pattern grooves related to forming conductor wiring patterns in semiconductor wafers or substrates. Ahmad and Masahiro either combined together or considered invidually fail to show all of the limitations of independent claim 1, from which claims 2-3 depend. Thus, the Office Action fails to establish a case of *prima facie* obviousness for dependent claims 2-3 as being unpatentable over Ahmad in view of Masahiro, and it is respectfully requested that the rejection of claims 2-3 under 35 U.S.C. § 103(a) over Ahmad in view of Masahiro be withdrawn in the next Office Action.

ITEM 4: Rejection of claims 1-5 under 35 U.S.C. § 103(a) over Lin in view of Ahmad—Not

in Compliance with 37 CFR § 1.104(c) (2)

In the January 11, 2005 Office Action, it is unclear as to which references applied to the rejection of claims 1-5 are to be considered the best references, and which rejections of claims 1-5 present all valid grounds of rejection, because claims 1-5 are rejected in piecemeal, i.e., twice by two distinct sets of applied art, creating an undue multiplication of references; the Office Action "is not called upon to cite *all* references that may be available, but only the 'best.'" And "multiplying references ... adds to the burden ... of prosecution and should therefore be avoided." (See MPEP 904.03, and MPEP 707.07(g)).

On the merits, the Office Action in referring to Lin (Figures 12b-12g), asserts that "Lin et al. teaches a method of forming a conductor wiring pattern comprising the steps of: forming a first insulating layer (4) on a surface of a substrate (1) ...." This is incorrect, the disclosure depicted in either Lin (Figures 12b-12g) as cited in the Office Action or a discussion of these figures found in Lin (¶¶¶[48-60]) fails to show all of the recited limitations of the forming element of claim 1, i.e., of "forming a first insulating layer on a surface of a substrate ...." Contrary to the Office Action assertion, Lin (Figures 12b-12g; and ¶¶¶[48-60]) shows "metal layers 3" formed over a "silicon substrate 1 ...."

The Lin reference does not show all of the limitations of the "light-exposing" element of claim 1, which as amended recites:

> light-exposing and developing the second insulating layer to form pattern grooves, each having sidewalls and a bottom so that the first insulating layer is exposed at the bottom of each pattern groove ...."

(claim 1, lines 5-7). A review of Lin (Fig. 12b) compared with Fig. 1(c) of the instant invention shows that in Lin (Fig. 12b), the bottom of each of the wiring pattern grooves is not the top surface of the first insulating layer, i.e., "passivation layer 4", in this case Lin, at the bottom of "pattern 7' ", shows "points of contact 6, such as bonding pads" exposed, not the first "passivation layer 4."

The Lin reference does not show all of the limitations of the "forming a plating seed layer" element of claim 1, which as amended recites:

> forming a plating seed layer on the second insulating layer including inner surfaces of the pattern grooves and then forming a resist pattern on the plating seed layer except for portions of the pattern grooves of the second insulating layer so that the seed layer only on the sidewalls and the bottom of the pattern

groove is exposed ....

(claim 1, lines 8-11). A review of Lin (Fig. 12d; and FIG. 12e) compared with Fig. 1(e) and Fig. 1(f) of the claimed invention reveals that Lin (Fig. 12d; and FIG. 12e) does not show the limitation of "forming a resist pattern on the plating seed layer except for portions of the pattern grooves of the second insulating layer so that the seed layer only on the sidewalls and the bottom of the pattern groove is exposed ...." In contrast, Lin (Fig. 12d; and FIG. 12e) shows forming a resist pattern on only portions of the second insulating layer surface, i.e., polymer 5, while other portions of the insulating layer surface, i.e., polymer layer 5 are not covered with a resist pattern.

Lin fails to show all of the limitations of claim 1 as amended. And, as discussed in Item 2 above concerning the rejection of claims 1, and 4-5, Ahmad also fails to show all of the limitations of claim 1. Lin and Ahmad either combined together or considered invidually fail to show all of the limitations of claim 1. Thus the Office Action fails to establish a case of *prima facie* obviousness for independent claim 1 as being unpatentable over the applied art Lin in view of Ahmad.

Dependent claims 2-5 depending from independent claim 1 or subsequent base claims are patentable over the applied art of record Lin in view of Ahmad for at least the same reasons that independent claim 1 is patentable over the applied art Lin in view of Ahmad; furthermore, Lin and Ahmad either combined together or considered invidually fail to show all of the limitations of dependent claims 2-5.

It is respectfully requested that the rejection of claims 1-5 under 35 U.S.C. § 103(a) over Lin in view of Ahmad be withdrawn in the next Office Action.

Furthermore, the applied art of record fails to show all of the limitations of newly added independent claim 6 and dependent claims 7-9 for the same reasons discussed above concerning the rejection of claim 1, because independent claim 6 includes pattern groove forming limitations similar to pattern groove limitations of independent claim 1.

It is respectfully requested that this Amendment After Final be entered in the above-referenced application and that a notice of allowance be issued for claims 1-9 in the next Office Action.

If there are any additional fees associated with filing of this Amendment After Final, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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Date: April 21, 2005

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